



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

cl

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/642,658	08/19/2003	Hidenori Sato	XA-9519A	3468

181 7590 01/28/2004

MILES & STOCKBRIDGE PC  
1751 PINNACLE DRIVE  
SUITE 500  
MCLEAN, VA 22102-3833

EXAMINER

PERKINS, PAMELA E

ART UNIT PAPER NUMBER

2822

DATE MAILED: 01/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

10/642,658

Applicant(s)

SATO ET AL.

Examiner

Pamela E Perkins

Art Unit

2822

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 19 August 2003.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 19 August 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. §§ 119 and 120

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☒ Certified copies of the priority documents have been received in Application No. 09/905,887.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 13) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.
- a) ☐ The translation of the foreign language provisional application has been received.
- 14) ☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

### Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 8/19/2004 . 6) ☐ Other: \_\_\_\_\_

### DETAILED ACTION

This office action is in response to the filing of the application papers on 19 August 2003. Claim 1 is pending.

#### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ohta et al. (6,268,295) in view of Egawa (6,118,145).

Ohta et al. discloses a method of making a semiconductor device where a first silicon nitride layer (16) is formed by chemical vapor deposition (CVD) over a substrate (11), forming a gate electrode (15g) over the substrate (11), forming a second silicon nitride layer (21) by CVD over the gate electrode (15g) anisotropically etching the second silicon nitride layer (21) to form sidewall spacers (21s) adjacent to the gate electrode (15g), forming a third silicon nitride layer (42) by CVD over the gate electrode (15g), forming a silicon oxide layer (43) over the third silicon nitride layer (42) and etching a contact hole (48) through the third silicon nitride layer (42) and the silicon oxide layer (43) (col. 7, line 25 thru col. 11, line 30). Ohta et al. further disclose forming the first, second and third silicon nitride layers at three different flow rates to have three different etching rates, wherein the third nitride layer has the largest flow rate and the

second silicon nitride layer flow rate is the smallest (col. 4, line 40 thru col. 7, line 24). Ohta et al. disclose forming the silicon nitride layers in CVD chamber (1) where a single wafer (10) is placed in the chamber (1), inserting ammonia and monosilane or dichlorosilane gases into the chamber (1) and heat the wafer (10) with a heating lamp (4), wherein the walls of the chamber (1) stay cool and only the vicinity around the wafer (10) is heated (Fig. 1; col. 4, lines 15-62). Ohta et al. do not disclose a low pattern density region and a high pattern density region.

Egawa discloses a semiconductor device where a substrate (1) has a low density peripheral pattern region and a high density memory cell pattern region, wherein a plurality of gate electrodes is formed on the substrate (1) and a dielectric layer (18) comprising a silicon nitride layer and silicon oxide layer is formed over the gate electrodes. Egawa further discloses a difference in the thickness between the peripheral region and the memory cell region (col. 2, lines 32-53; col. 5 line 8 thru col. 6 line 47).

Since Ohta et al. and Egawa are both from the same field of endeavor, a manufacturing method of a semiconductor integrated circuit device, the purpose disclosed by Egawa would have been recognized in the pertinent art of Ohta et al. Therefore, it would have been obvious to one ordinary skill in the art at the time the invention was made to modify Ohta et al. by having a low pattern density region and a high pattern density region as taught by Egawa for the purpose of ensuring the capacitance of the memory cells (col. 1, lines 13-23).


***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pamela E Perkins whose telephone number is (571) 272-1840. The examiner can normally be reached on Monday thru Friday, 9:00am to 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

PEP

  
AMIR ZARABIAN  
UNITED STATES PATENT EXAMINER  
TECHNOLOGY CENTER 2800